

High Pressure Sensor Digital Output – 150°C







- Compact Absolute Pressure Sensor (0.50" Hex)
- 1ms Response Time
- Pressure/temperature read-out
- 1.0% Total Error Band
- Digital Output (14 Bit) SPI
- 500 5,000 PSI Pressure Range
- Media Harsh Liquid, Air, & Gas

DESCRIPTION

The APS74 is a pressure transducer manufactured for a high operating temperature range for the most challenging of applications. This silicon pressure transducer was designed for demanding industrial and commercial applications. The stainless steel media isolated port design allows for pressure measurement of liquid or gas media.

The APS74 series utilizes MEMS piezo-resistive sensors pressurized on the passive backside of the SS diaphragm which has superior long term stability and accuracy (.15% Linearity).

The design is simple and provides value for OEM customers. Please contact us for custom design availability.

APPLICATIONS

- Military/Aerospace
- Industrial Automation
- HVAC
- Automotive Engine
- Compressor
- Pneumatic

Maximum Environmental Ratings

Operating Temperature	0°C to	150°C
Storage Temperature Range	55°C to	175°C

Proof	pressure	 	 	3x	full	scale	pressi	are
Burst	pressure	 	 	5x	full	scale	pressi	ıre



Package

The one piece body design is made of 316L stainless steel, which allows for easy manufacturability and long term stability.

Stability

The silicon MEMS pressure sensor has a Pyrex base and is mounted to a ceramic base and sealed into the SS housing. Flexible die attach materials help reduce the mechanical stress which results in greater stability over time and temperature.

Additional stability is gained from factory stabilization of all sensors.

Pressure port

The thread is 5/16-24 UNF.

Media

The pressure port is tolerant to most media including but not limited to oil, air, gas, some corrosive media, and salt water.

Wetted parts

The wetted surfaces are composed of 316L stainless steel.

Pressure Range

The standard pressure ranges are 500 - 5,000. Custom pressure ranges are available for OEM customers.

Wiring

The electrical connection wires are 28 AWG Teflon. The standard length is 12" but can be changed upon request. The wires can easily be attached to a connector or soldered directly to a board.

APS74 Digital Output Operational Characteristics

PARAMETER	SYMBOL	Min	Тур	Max	UNITS
Supply Voltage	Vdd	2.7	5	5.5	V
Operating Temperature	Ts	0		150	С
Supply Current (Note 1)	I _{DD}	70	120	2500	μΑ
Sleep Mode Supply Current	stdby		.5	32	μΑ
		Α	ccuracy		
Total Error Band		-1.0		1.0	%Full Scan
Non-Linearity (Note 2)		1		.1	%Full Scan
Temperature Error (Null and Span) (Note 3)		-1	.5	1	С
Response Time	t _R	1	2	20	ms
		Analo	og-to-Digital		
Resolution	ADC		14		Bits
Temperature Resolution			0.1		С
	-	SP	I Interface		
Input Low Level	Vin_low	0		.2	Vdd
Input High Level	Vin_high	.8		1	Vdd
Output Low Level	Vo_low			.1	Vdd
Load Capacitance @SDA	Csda @400khz			200	pF
Pull-Up Resistor	R ^{12C_PU}	500			Ω
Input Capacitance (each pin)	CI2C_In			10	pF

 $V_{+} = 5V, V_{-} = 0V, Temperature = 25^{\circ}C$

Notes: 1) Measured at zero pressure. 2) Defined as best straight line 3) Measured from 0°C to 150°C.

Electrical Pin Configuration (Digital [SPI])

Yellow - SCL/SCLK Green - SDA/MISO White- INT/SS Red- V+ Black GND

Figure 1

SPI – Digital Interface

Digital Interface – SPI

SPI is available only as half duplex (read-only from the APS74). The factory default is negative edge detect with a clock frequency of 4 MHz.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCLK clock frequency (4MHz clock)	f _{SCL}	50		800	kHz
SCLK clock frequency (1MHz clock)	f _{SCL}	50		200	kHz
SS drop to first clock edge	t _{HDSS}	2.5			μs
Minimum SCLK clock low width	t _{LOW}	0.6			μs ¹
Minimum SCLK clock high width	t _{HIGH}	0.6			μs ¹
Clock edge to data transition	t _{clkD}	0		0.1	μs
Rise of SS relative to last clock edge	t _{suss}	0.1			μs
Bus free time between rise and fall of SS	t _{BUS}	2			μs

¹ Combined low and high widths must equal or exceed minimum SCLK period.

Table 1



Figure 2

SPI Read

SPI Read Operations

For simplifying explanations and illustrations, only falling edge SPI polarity will be discussed in the following sections. The SPI interface will have data change after the falling edge of SCLK. The master should sample MISO on the rise of SCLK. The entire output packet is 4 bytes (32 bits). The high bridge data byte comes first, followed by the low bridge data byte. Then 11 bits of corrected temperature (T[10:0]) are sent: first the T[10:3] byte and then the {T[2:0],xxxx} byte. The last 5 bits of the final byte are undetermined and should be masked off in the application. If the user only requires the corrected bridge value, the read can be terminated after the 2nd byte. If the corrected temperature is also required but only at an 8-bit resolution, the read can be terminated after the 3rd byte is read.



Figure 3

Part Number Configuration

Standard Part Numbers

Model	Pressure Range PSI	Туре	Max Over Pressure
APS74-0.5K	500	Abs/Gage	900
APS74-1K	1000	Abs/Gage	3000
APS74-3K	3000	Abs/Gage	5000
APS74-5K	5000	Abs/Gage	7000



Figure 4

PSI	PSI	PSI	PSI	% Output	Decimal	Hex
0	0	0	0	0	0	0 x0000
50	100	300	500	10	1638	0 x 0666
100	200	600	1000	20	3277	0 x 0CCD
150	300	900	1500	30	4915	0 x 1333
200	400	1200	2000	40	6553	0 x 1999
250	500	1500	2500	50	8192	0 x 2000
300	600	1800	3000	60	9830	0 x 2666
350	700	2100	3500	70	11468	0 x 2CCC
400	800	2400	4000	80	13106	0 x 3332
450	900	2700	4500	90	14745	0 x 3999
500	1000	3000	5000	100	16383	0 x 3FFF

Table 2



Temp C	% Output	Decimal	Hex
0	0	0	0 x0000
25	13	263	0 x 0107
50	26	525	0 x 020D
75	38	788	0 x 0314
100	51	1050	0 x 041A
125	64	1313	0 x 0521
150	77	1575	0 x 0627
175	90	1838	0 x 072E
195	100	2047	0 x 07FF



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